PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference 03F016-PCT	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/JP 03/07672	International filing date *(day/month/year)* 17.06.2003	Priority date *(day/month/year)* 19.06.2002
International Patent Classification (IPC) or both national classification and IPC G06F12/02		
Applicant TOKYO ELECTRON DEVICE LIMITED et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 6 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the opinion
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
29.07.2004	28.12.2004
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized Officer Weber, R Telephone No. +49 89 2399-2655

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/JP 03/07672

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:

Description, Pages

1-41	as originally filed

Claims, Numbers

3 (part), 4-23, 24 (part), 30 (part), 31	as originally filed
1, 2, 3 (part), 24 (part), 25-29, 30 (part)	received on 02.08.2004 with letter of 29.07.2004

Drawings, Sheets

1-16	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).

   ☐ the language of publication of the international application (under Rule 48.3(b)).

   ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   ☐ contained in the international application in written form.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority in written form.

   ☐ furnished subsequently to this Authority in computer readable form.

   ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   ☐ the description, pages:

   ☐ the claims, Nos.:

   ☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)).

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	
	No:	Claims	1-31
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1-31
Industrial applicability (IA)	Yes:	Claims	1-31
	No:	Claims	

2. Citations and explanations

   see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Claim 1

The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claim 1 is not new in the sense of Article 33(2) PCT.

The following documents show the features of claim 1 as indicated in the table.

document	passages page(lines) or column(lines)	comments	JP03/07672 claim(lines)
D1 : WO-A-0049488	fig.1-4; 20(14-25); 27(34)-28(12)	fig.2 concerns a controller 8 to control a flash memory 6, which is divided into blocks 4, each block divided into physical pages such as 1-3; each physical page includes the host sector data 1a and a header 1b with parameters 22 such as the logical sector address LA	1(4-8)
	2(6-8); 3(4-12); 3(12-18); 9(31)-10(27)	a translation table SAT correlates a logical address of a sector to a physical sector address; the SAT is stored in SAT blocks of the flash memory but the most recently used translations are first maintained as lists WSL,WBL in a volatile memory SRAM 13 of the controller 8 until a whole SAT block is written into the flash memory	1(9-11)
	2(9-16)	when writing to the flash memory, a write pointer WP maintains the write position of a next available sector address in a block;	1(12-14)
	10(29)-11(8); 54(1-32)	at initialisation the write pointer WP and that part WSL,WBL of the address translation table SAT which is located in the volatile memory SRAM 13 are reconstucted by scanning the logical sector addresses LA in the page headers through the flash memory	1(15-19)
	2(17-29)	after writing data into the selected sector address the translation table is updated at the logical address by the physical address of the new sector indicated by the write pointer WP	1(19-23)
D2 : GB-A-2 291 991	fig.2 6(9-14,18-22)	a flash memory 5 may be divided into erase blocks 32 each divided again into sectors	1(4-8)
	5(25-28); 8(22-23)	a table is used to translate a logical sector address into a physical sector address	1(9-11)

	7(29)-8(5)	a write pointer specifies the address of an empty physical sector where a next data is to be written	1(12-14)
		the details of the creation of the address translation table is not shown; but reconstructing such a table by scanning the logical addresses stored in the sector headers is the most usual (see D1,D3,D4,D5)	1(15-19)
	7(32)-8(2); 8(22-23)	after writing a sector the table is updated	1(19-23)
D3 : EP-A-0615184	fig.2,3 5(46-54)	a flash memory 34 is divided into erasable blocks, each containing 8 accessible pages called sectors	1(4-8)
	9(37)-10(3); 18(1-18); 6(37-49);	at initiation a translation table is reconstructed which correlates a physical address of a sector to a logical sector address called reverse pointer, which is stored with each sector in the flash memory	1(9-19)
	5(1-14)	writing of a sector is done according to the dynamic sector allocation method to write data into a new empty sector whereby the correlation between the new physical address and the logical address RBA of the sector is maintained in the translation table	1(20-23)
D4 : US-A-5 459 850	fig.1; 20(35-38)	fig.1 concerns a controller to control a flash memory 27, which is divided into erasable blocks each divided into pages called sectors;	1(4-8)
	Fig.3B; 17(31-37) 19(59-62)	a translation table correlates a logical address LSN of a page to a physical address PFA	1(9-11)
	fig.3c 20(53-67)	when writing to the flash memory, a pointer maintains the last write position to select a next available sector address in a block;	1(12-14)
	21(45-47)	at power up the translation table is recreated from header information stored in the flash memory	1(15-19)
	fig.3c 20(67)-21(2)	after writing data into the selected sector address the translation table is updated by the physical address PFA at the logical address LSN	1(19-23)
D5 : US-A-6 477 616 = JP2000305839	fig.2	a flash memory is divided into blocks each divided into pages	1(4-8)
	fig.5	a table BPT is used to translate the logical block address into a corresponding physical block address	1(9-11)
	23(65)-24(50)	a write pointer cyclically points to empty blocks into the flash memory	1(12-14)

	fig.6; 15(1-33); 11(1-11)	at initiation the translation table BPT is reconstructed from logical block addresses, which are stored with each block in the flash memory	1(15-19)
	20(12-36)	after writing into a new page the table BPT is updated	1(19-23)

Independent claims 26,29

Independent claims 26,29 only contain features corresponding to the features of claim 1 and therefore the same objections hold.

Dependent claims

Dependent claims 2-25,27,28,30,31 do not contain any features which, in combination with the features of any claim to which it/they refers/refer, meet the requirements of the PCT in respect of novelty and/or inventive step, the reasons being that these features are prior art as follows:

claim	document passages	comment
2,5,27,30	D2, 8(19-22)	prior to erasure of a block, valid data in sectors are relocated
	D1, 7(17-21)	valid sectors in a block (COB) are relocated into another empty block before the block COB is erased
	D3, 9(15-23)	prior to erasing it is determined whether a sector should be copied
	D4, 20(43-51)	prior to erasure of a block, the non-dirty sectors are restored into a clean block
3,28,31	D2, 8(15-18)	a block is erased when the number of empty blocks is low
	D3, 7(48-54)	
4,6,7	D1, 7(2-23);57(30)-58(12);26(1-12)	the oldest block having obsolete data is erased in a circular manner
8	D3, 9(15-23)	only data in sectors where a reference exist in the translation table are recopied into a new block
9,6	D2, 8(2-5;6-15);	write and erase pointers are cyclic
	D1, 4(6-21)	
10,11	D1-D5	the translation table is also used for readout
12-14	D4, 17(34-66);fig.2B,3B	the translation table uses only the upper bits of the addresses
15	D5, 11(17-35);19(6-25)	the translation table uses only the lower bits of the addresses
16-25	D1, 3(12-32)	the translation table may also be stored in the flash memory

CLAIMS

1. A memory device characterized by comprising:

a memory (11) including a plurality of memory blocks for storing data to which physical addresses are allocated;

a translation table memory (123) which stores an address translation table showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages;

a pointer memory (123) which specifies an empty page in a data storable state from among said pages and stores a write pointer indicating a physical address of said specified empty page; and

a controller (12, S311, S314) which, when to-be-written data and a logical address are supplied to said memory device, writes said to-be-written data in the empty page indicated by said write pointer, and renews said address translation table in such a way as to show a correlation between the physical address of that empty page and said logical address.

2. The memory device according to claim 1, characterized in that said controller (12) designates memory blocks from which data is to be erased from among those memory blocks which have data stored therein (S501), and

discriminates whether data stored in said designated memory blocks is valid or not, for each of those pages which constitute said designated memory blocks, transfers that data which has been discriminated as valid to another memory blocks (S502, S506), and erases that data which is stored in said designated memory blocks (S503).

3. The memory device according to claim 2, characterized in that said controller (12) discriminates whether or not the number of those memory blocks which do not have data stored therein becomes a number which does not satisfy a predetermined condition (S317), and

designates memory blocks from which data is to be erased from among data-storing

lower digits of the physical address of a page storing that data which constitutes said empty block table (S107), and reads at least a part of said empty block table from that page which is included in pages each having a physical address whose lower digits are specified by said empty block table pointer and which has a physical address whose upper digits lie in said range (S308).

25. The memory device according to claim 24, characterized in that said controller (12) specifies that page in which a to-be-renewed part in said stored empty block table is stored from among those pages which have said empty block table stored therein, and reads out only that part which is stored in said specified page.

26. A memory managing method for managing a plurality of memory blocks for storing data to which physical addresses are allocated, characterized in that

an address translation table showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages is stored (S105),

an empty page in a data storable state is specified from among said pages and a write pointer indicating a physical address of said specified empty page is stored (S107), and

when to-be-written data and a logical address are supplied, said to-be-written data is written in the empty page indicated by said write pointer, and said address translation table is renewed in such a way as to show a correlation between the physical address of that empty page and said logical address (S311, S314).

27. The memory managing method according to claim 26, characterized in that memory blocks from which data is to be erased is designated from among those memory blocks which have data stored therein (S501), and

it is discriminated whether data stored in said designated memory blocks is valid or not, for each of those pages which constitute said designated memory blocks, that data which has been discriminated as valid is transferred to another memory blocks, and that

data which is stored in said designated memory blocks is erased (S502, S506, S503).

28. The memory managing method according to claim 27, characterized in that it is discriminated whether or not the number of those memory blocks which do not have data stored therein becomes a number which does not satisfy a predetermined condition (S317), and

when it is discriminated that the number of said memory blocks which do not have data stored therein has become the number which does not satisfy said predetermined condition, a memory block from which data is to be erased is designated from among data-storing memory blocks (S501).

29. A program for allowing a computer (121), connected to a memory (11) including a plurality of memory blocks for storing data to which physical addresses are allocated, to function to:

store an address translation table showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages (S105);

specify an empty page in a data storable state from among said pages and store a write pointer indicating a physical address of said specified empty page (S107); and

when to-be-written data and a logical address are supplied to said computer, write said to-be-written data in the empty page indicated by said write pointer and renew said address translation table in such a way as to show a correlation between the physical address of that empty page and said logical address (S311, S314).

30. The program according to claim 29, characterized in that said program designates memory blocks from which data is to be erased from among those memory blocks which have data stored therein (S501), and

discriminates whether data stored in said designated memory blocks is valid or not, for each of those pages which constitute said designated memory blocks, transfers that data which has been discriminated as valid to another memory blocks, and erases that data

CLAIMS

1. (Amended) A memory device characterized by comprising:

a non-volatile memory (11) including a plurality of memory blocks for storing data to which physical addresses are allocated, each of said blocks including physical pages, each of said physical pages including a logical page and a redundancy portion;

a translation table memory (123) which stores an address translation table (BPT) showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages;

a pointer memory (123) which specifies an empty page in a data storable state from among said pages and stores a write pointer (BSI) indicating a physical address of said specified empty page; and

a controller (12, S311, S314) which, when this memory system is activated, performs initializing process in which reads data from the redundancy portions of said non-volatile memory and prepares the address translation table in said translation table memory and the write pointer in said pointer memory, when to-be-written data and a logical address are supplied to said memory device, writes said to-be-written data in the empty page indicated by said write pointer, and renews said address translation table in such a way as to show a correlation between the physical address of that empty page and said logical address.

2. The memory device according to claim 1, characterized in that said controller (12) designates memory blocks from which data is to be erased from among those memory blocks which have data stored therein (S501), and

discriminates whether data stored in said designated memory blocks is

valid or not, for each of those pages which constitute said designated memory blocks, transfers that data which has been discriminated as valid to another memory blocks (S502, S506), and erases that data which is stored in said designated memory blocks (S503).

3. The memory device according to claim 2, characterized in that said controller (12) discriminates whether or not the number of those memory blocks which do not have data stored therein becomes a number which does not satisfy a predetermined condition (S317), and

designates memory blocks from which data is to be erased from among data-storing

lower digits of the physical address of a page storing that data which constitutes said empty block table (S107), and reads at least a part of said empty block table from that page which is included in pages each having a physical address whose lower digits are specified by said empty block table pointer and which has a physical address whose upper digits lie in said range (S308).

25. The memory device according to claim 24, characterized in that said controller (12) specifies that page in which a to-be-renewed part in said stored empty block table is stored from among those pages which have said empty block table stored therein, and reads out only that part which is stored in said specified page.

26. (Amended) A memory managing method for managing a non-volatile memory having a plurality of memory blocks for storing data to which physical addresses are allocated, and each of said memory blocks including physical pages, each of said physical pages including a logical page and a redundancy portion, characterized in that

said method comprises the steps of :

when said non-volatile memory is activated, reading data from the redundancy portions of said non-volatile memory and preparing an address translation table showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages and a write pointer indicating a physical address of an empty page,

receiving to-be-written data and logical address; and

when to-be-written data and a logical address are supplied, writing said to-be-written data in the empty page indicated by said write pointer, and said address translation table is renewed in such a way as to show a correlation between the physical address of that empty page and said logical address

(S311, S314).

27. (Amended) The memory managing method according to claim 26, characterized in that memory blocks from which data is to be erased is designated from among those memory blocks which have data stored therein (S501), and

discriminating whether data stored in said designated memory blocks is valid or not, for each of those pages which constitute said designated memory blocks, transferring that data which has been discriminated as valid to another memory blocks, and erasing that

data which is stored in said designated memory blocks (S502, S506, S503).

28. (Amended) The memory managing method according to claim 27, characterized in that discriminating whether or not the number of those memory blocks which do not have data stored therein becomes a number which does not satisfy a predetermined condition (S317), and

when it is discriminated that the number of said memory blocks which do not have data stored therein has become the number which does not satisfy said predetermined condition, designating a memory block from which data is to be erased from among data-storing memory blocks (S501).

29. A program for allowing a computer (121), connected to a memory (11) including a plurality of memory blocks for storing data to which physical addresses are allocated, to function to:

store an address translation table showing a correlation between physical addresses of pages constituting each of said memory blocks and logical addresses of said pages (S105);

specify an empty page in a data storable state from among said pages and store a write pointer indicating a physical address of said specified empty page (S107); and

when to-be-written data and a logical address are supplied to said computer, write said to-be-written data in the empty page indicated by said write pointer and renew said address translation table in such a way as to show a correlation between the physical address of that empty page and said logical address (S311, S314).

30. The program according to claim 29, characterized in that said program designates memory blocks from which data is to be erased from among those memory blocks which have data stored therein (S501), and

discriminates whether data stored in said designated memory blocks is

valid or not, for each of those pages which constitute said designated memory blocks, transfers that data which has been discriminated as valid to another memory blocks, and erases that data